EE/CprE/SE 4910 WEEKLY REPORT 6

3/21/2026 – 3/27/2026

Group number: SD26-10

Project title: Open-sourced Radio Microcontroller for Fabrication

Client &/Advisor: Henry Duwe duwe@iastate.edu

Client/Company/Organization: ISU; ECPE

Team Members:

- ***Zane Salti***
- ***Jackson Doyle***
- ***Daniel Pytel***
- ***Tyler Bibus***
- ***Aiden Han-Lindemyer***
- ***Parker Pederson***
- ***Akash Gojuru***
- ***Seth Klaassen***

Weekly Summary:

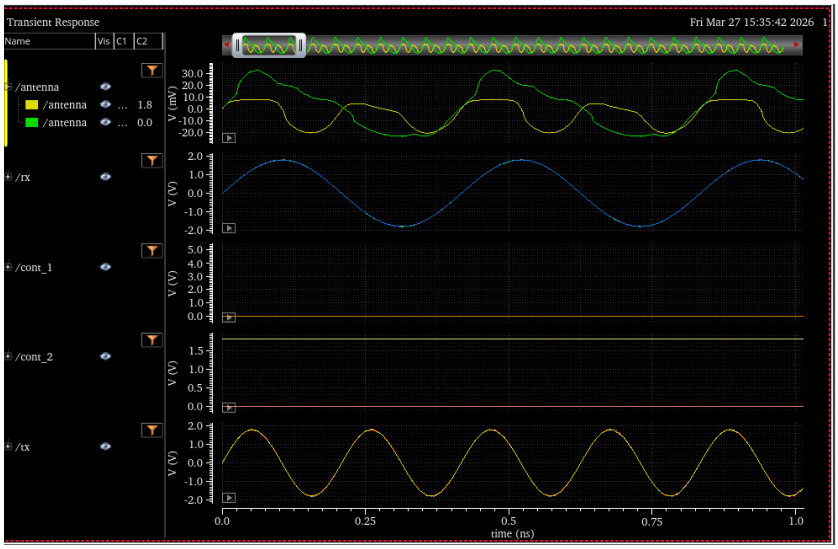
Examined additional testing methods including using an fpga PLL to generate an output. Started PCB project for antenna, ASIC mounting, and power delivery.

Digital Side:

The digital team was focused on the digital simulation this week command support increased from one command to 15 commands. A debug mode was added to the simulation. Bumble and Babble sim integration was started, it still requires some debugging due to disconnection issues. Wrote simulation code for CRC, PDU packet forming, and whitening.

Analog Side:

Evaluated circumstances for creation of the VCO on chip. Created contingency plan to move the VCO off chip if the design is shown to be infeasible. Inductors of SKY130 are extremely large. Creates floor planning problems. Began evaluation of the singular SKY130 inductor Pcell for feasibility. PDK was imported into cadence to allow for easier schematic design. RF switch schematic was created and underwent initial testing. Results were mixed, it did function but had large cross talk.

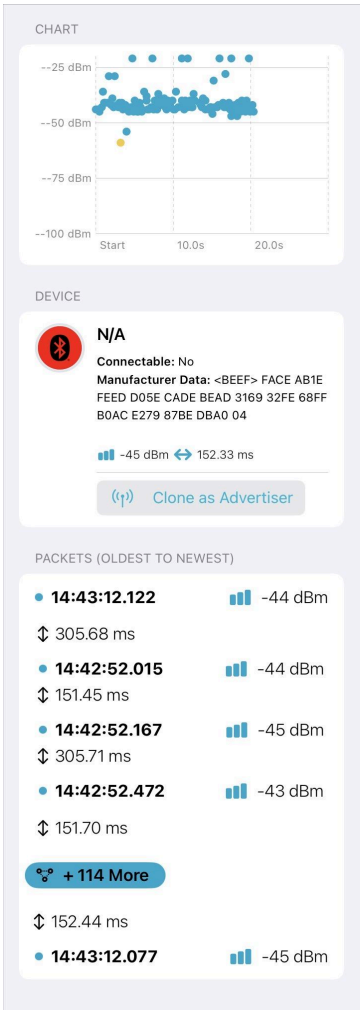


Began simulink setup for the design of the entire analog end.

Past week accomplishments

- Zane Salti:

  Got BLE advertisement going using nRF52840's radio peripheral. Disabled the radio's auto-whitening and auto-CRC so to use/test my own whitening and CRC implementation and to operate the radio at a more lower level.

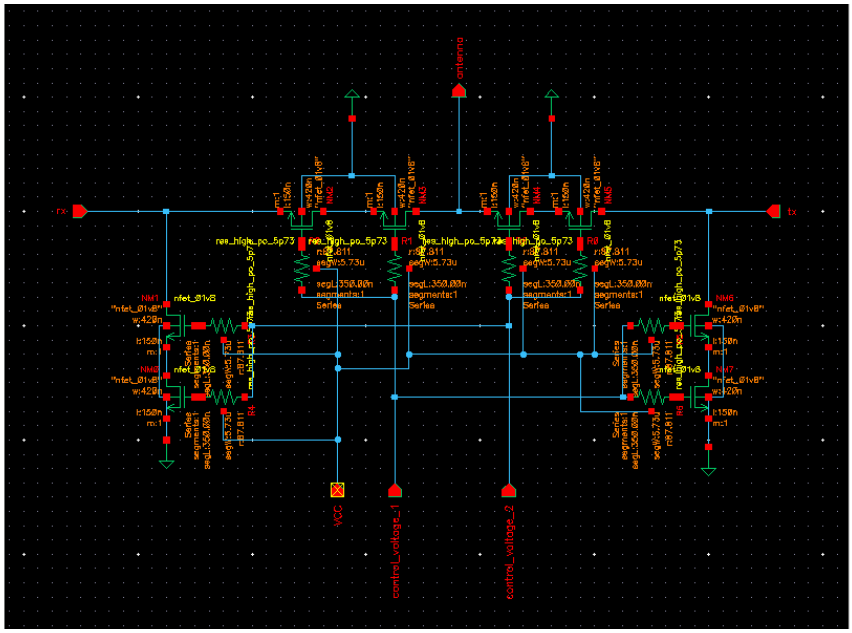


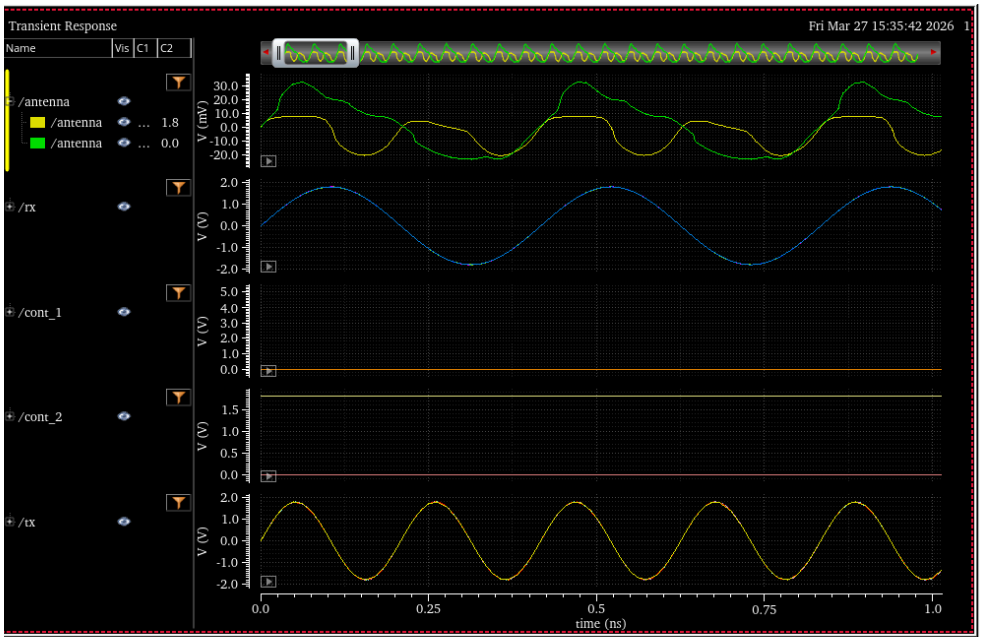
  Advertising packets show up on a tablet device (shown on left).

  Got started with designing a PCB to interface with the FPGA's transceiver, but rethinking some of it. Found out that the UltraScale+ board available to us has SMA connectors hooked up to transceivers which can be used over the SFP connectors.

  Hardware serializer written (but needs to be tested).

- Jackson Doyle:
    - Implementation of VCO model in MATLAB
    - Feasibility analysis for VCO realization
    - Narrowed down choices for VCO type.
- Daniel Pytel:
    - General PLL simulation in MATLAB
    - Cadence operation (mostly)
- Tyler Bibus:
    - Completed general admin related tasks relating to documents and planning.
    - Connected BabbleSim (Phy) with BumbleSim (Host) with support for advertising.
- Parker Pederson:
    - Added support for 8 commands in HCI simulation
    - Added debug mode for the simulation to allow for faster implementation
    - Small refactor for hci simulation
- Akash Gojuru: Wrote C code for the top-level Link Layer, including implementation of CRC, PDU handling, and data whitening. Conducted testing for advertising functionality using a manually configured device address.
- Seth Klaassen: modeled the RF switch in skyworks130 process, using the 1v8 nmos transistors. Still haven't properly tuned the widths on the transistors. Current gain is roughly -100 v/v which is very bad. As you can see in the waveforms below there is also some bleeding between the two channels making the output waveform not only verry small but also incredibly noisy and distorted.





- Aiden Han-Lindemyer
    - Resolved advertiser compatibility issue blocking host simulation
    - Implemented 5 missing LE advertising HCI commands in controller simulation
    - Fixed capability bitmask
    - Worked on error handling for unsupported classic buffer commands

Pending issues

- Zane Salti: Need to test HDL serializer.
- Jackson Doyle:
    - Need to finish MATLAB/Simulink implementation of the high level parameters, choose antenna, and allocate gain, noise, etc.
- Daniel Pytel:
    - Cadence is suffering from some file directory issues
- Tyler Bibus:
    - Managing design document.
    - Still need to verify the validity of the simulation environment.
- Aiden Han-Lindemyer:
    - Still need to document commands and fit them into project scope
- Akash Gojuru: Still working on finishing the connection state machine for the Link Layer.
- Parker Pederson: Need to integrate bumble and babble into a singular simulation
- Seth Klaassen:rebalencing transistor widths

Time Tracking

NAME	Hours this week	HOURS cumulative

Zane Salti	6	43
Jackson Doyle	8	27
Daniel Pytel	5	22
Tyler Bibus	8	28
Aiden Han-Lindemyer	7	27
Parker Pederson	4	27
Akash Gojuru	7	26
Seth Klaassen	6	25

Comments and extended discussion

Plans for the upcoming week

- Zane Salti: Test HDL serializer, have serializer on fpga work with radio peripheral or get fpga transceiver running, and look at rf filters for a pcb to support a simple transceiver to antenna testing.
- Jackson Doyle:
    - Work on design doc and future planning. Task allocation/schedule.
    - Work on simulink PLL model, introduce specifics and possibly imitate parasitics.
    - Depending on progress, also implement the switching mechanism (by ideal operation using embedded simulink controls) to see how the overall transfer from link to antenna operates.
- Daniel Pytel:
    - Iron out any issues with Cadence
        - Get Git repository to play nicely with it
    - Further model components in Simulink
    - Hopefully obtain full schematic for system as preparation for another advisor meeting in the coming weeks
- Tyler Bibus:
    - Admin tasks:
        - Create Gantt chart for project
        - Redo design document segments based on advisor feedback
        - Organize overall project structure in a way to proliferate greater collaboration and improve communication.

    - Simulation Environment:
        - Verify current implementation regarding Bumble and Babble
        - Implement remaining HCI commands.
        - Explore and implement further decomposition of functions to better reflect future hardware implementation.
    - Digital Design:
        - Complete ChipForge tutorials on specific tools for digital implementation.
        - Decompose top level diagram further for hardware implementation based on simulation results.
- Aiden Han-Lindemyer:
    - Document commands in design document
    - Continue with HCI command support
    - Lightning Talk Preparation
- Parker Pederson:
    - Document register map for the hci
    - Increase HCI command support
    - Integrate babble and bumble sim
- Akash Gojuru: Understand how the BabbleSim interface files work and how they interact with the PHY layer simulation. Connect the Link Layer to BabbleSim and test it with a Zephyr central device to verify that advertising works correctly.
- Seth Klaassen: modeling in xschem and magic, allows for more options in device type and allows for parasitic calculations

Summary of weekly advisor meeting

- Top Level:
    - No notes, seems happy
- Design Document:
- Discussion on meeting with Neihart:
    - No feedback, Need to implement model in matlab to keep him happy most likely
- Zane:
    - Duwe is pretty sure that the FPGA Ultra Scale is janky and could work but is like stacking ladders on each other on wheels. We should ask Neihart about equipment options that might be easier to work with.
    - SFP Port is Fiber (Optical) which could cause issues
    - Duwe suggests a different approach, potentially a signal generator. If using Eval board it would be better to use SMA connector w/ 10 GHz pins.
    - Ask Neihart first.
- PHY:
    - For an off chip VCO we would need to also deliver a PCB (Which sounds fun TBH)
    - Found a great reddit post on r/chipDesign exploring RF SKY130 stuff
    - Reddit post dropped in ChipForge SDDEC26-10 Channel
    - Action on Neihart feedback, then meet again with him for more information
- Digital:

    - He likes the full simulator for the comparison.
    - Should get more hardware functionality completed.
    - Start focusing on translating the simulation and design to hardware.
- Admin:
    - Start breaking stuff down, subteams, improve organization and long-term planning with tables and charts.