EE/CprE/SE 4910 WEEKLY REPORT 8

4/4/2026 – 4/17/2026

Group number: SD26-10

Project title: Open-sourced Radio Microcontroller for Fabrication

Client &/Advisor: Henry Duwe duwe@iastate.edu

Client/Company/Organization: ISU; ECPE

Team Members:

- ***Zane Salti***
- ***Jackson Doyle***
- ***Daniel Pytel***
- ***Tyler Bibus***
- ***Aiden Han-Lindemyer***
- ***Parker Pederson***
- ***Akash Gojuru***
- ***Seth Klaassen***

Weekly Summary:

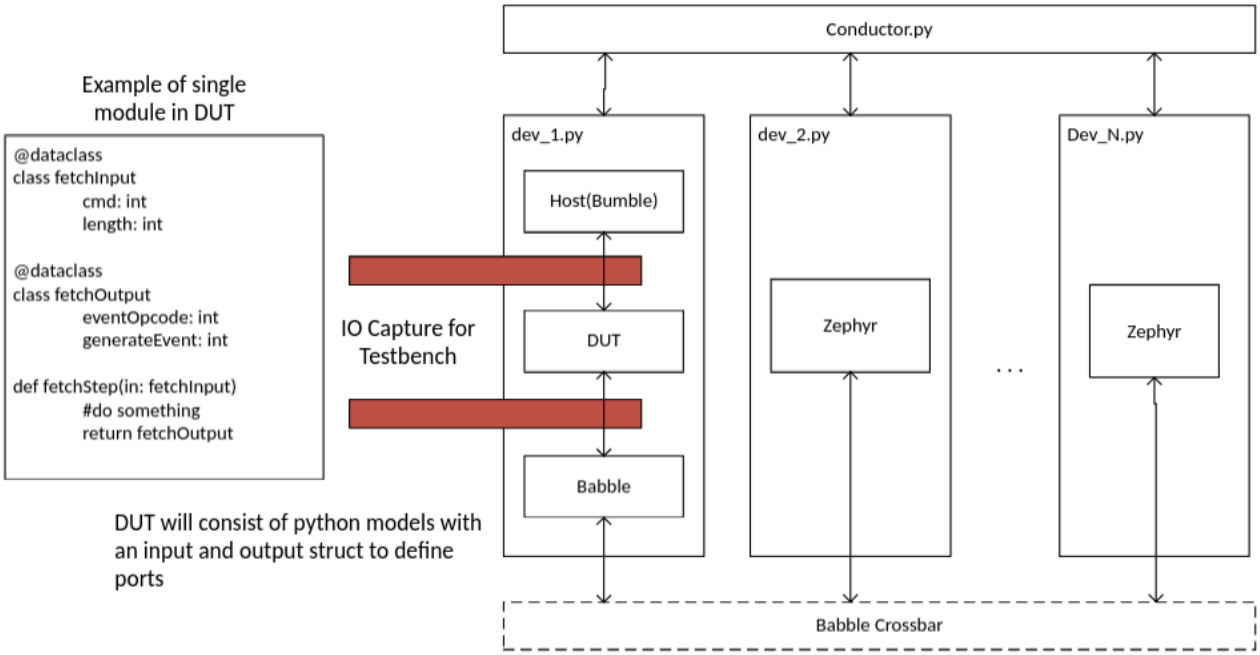
Digital Subteam:

The digital team has decided on a refactor of the current simulation approach to python with a more organized structure. This will allow for better debugging and further capabilities with third party libraries. The rational for this change is that Python will provide the following improvements:

- Easier logging
- Faster development
- Less cross language issues
- More flexibility in testing and future testbench development
- Better third party libraries

The unfortunate part about this change is that we are losing some progress as we need to rewrite sections of C as well as a new Device.py and Conductor.py. This is well worth the effort as it will result in a superior testing environment, likely sooner as well.

Below is the architecture of our new simulation environment.



Past week accomplishments

- Zane Salti:
  - Serializer verified and working
  - Explored a PLL and VCO that has an existing layout
  - Worked on setting up and getting the Ultrascale+ GTH transceiver configured as well as debugging it
- Jackson Doyle:
  - Continued work on simulink PHY
  - Reduced sim time to under a minute
  - Achieved expected TX and RX behavior for simple/ideal system conditions
- Daniel Pytel:
  - Sourced prospective VCO for tapeout to test Caravel platform
  - Researched Antennas
  - Secured space on ChipForge tapeout
  - Coordinated another external faculty meeting
- Tyler Bibus:
  - New sim structure created and assigned subtasks.
  - Basic device.py and conductor.py laid out in addition to sub modules
  - Git issue board for digital team progress tracking.
  - Design document problem statement & user section updated based on advisor feedback.
- Aiden Han-Lindemyer:
  - Refactored fetch module to aid in transition into new sim architecture.
  - Began implementation of new python modules
- Parker Pederson:

    - Basic integration of modules into device file
    - Designed new sim architecture
    - Completed Magic tutorials
    - Compared global 180 to the sky 130 process to gain insight into RF applications
- Akash Gojuru:
    - Successfully connected LL to the babblesim and able to the see advertising in the zephyr device central.
    - Implemented connection state and able to connect the LL to the central device.
    - Started working on the conductor.py

- Seth Klaassen:
    - Found the layout file for the VCO
    - After finding out that layout file had misplaced inductor had to rearrange components to fit it
    - Measured area of VCO and put it in terms of caravel package area and calculated around 4% space required for the VCO

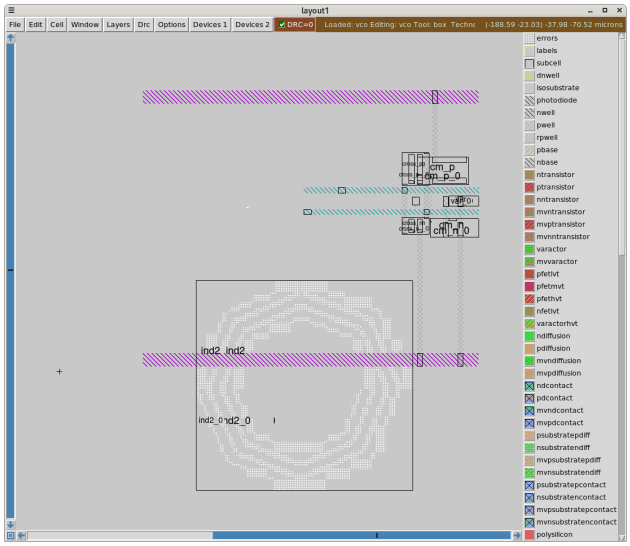


Figure 1: *Layout before modification*

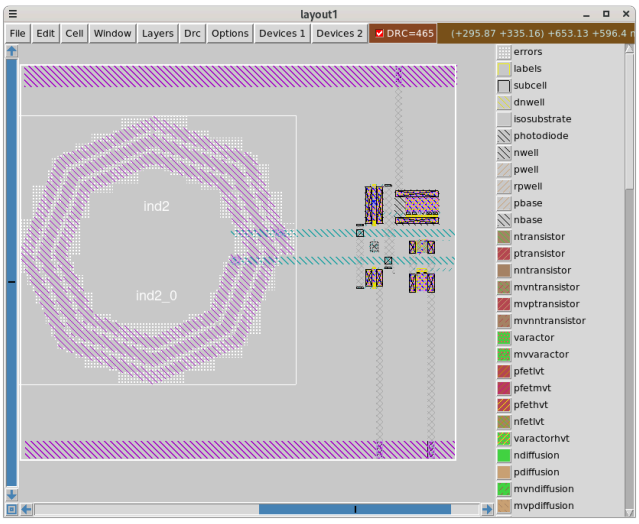


Figure 2: *Layout after modification*

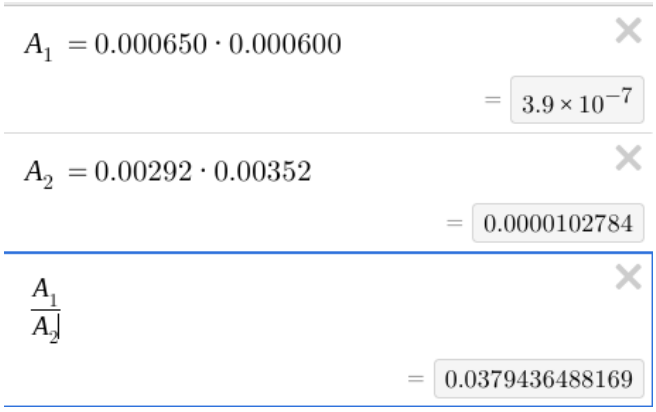


Figure 3: *Required percentage of the Caravel package space*

Pending issues

- Zane Salti: Transceiver needs further testing
- Jackson Doyle: Running into limits of efficient functionality in regards to simulink usage. Non-ideal and robust representation of the PHY has become difficult as simulation times are greatly increased
- Daniel Pytel: File/sourcing issues regarding tapeout VCO
- Tyler Bibus: Implementing modules in python, running into some issues with Bumble working as expected.
- Aiden Han-Lindemyer:
- Parker Pederson: New sim does not hook into bumble sim. The simulation thinks that the PTY is being written to but it is not.
- Seth Klaassen:
- Akash Gojuru: Had an issue that not able to transfer the data after connection

Time Tracking

NAME	Hours these two weeks	HOURS cumulative
Zane Salti	19	66
Jackson Doyle	15	50
Daniel Pytel	10	36
Tyler Bibus	11	45
Aiden	11	41

Han-Lindemyer		
Parker Pederson	13	43
Akash Gojuru	11	42
Seth Klaassen	14	44

Comments and extended discussion

Plans for the upcoming week

- Zane Salti: Further test and debug the transceiver as well as design a gaussian filter module and the required hardware to GFSK module the PLL in the transceiver to produce a proper BLE packet.
- Jackson Doyle:
    - Begin design work/implementation of phy components in toolchain assuming functional LC VCO down the line in october tapeout.
    - Simulink work
- Daniel Pytel:
    - Adjust Simulink system (following Neihart meeting)
    - Further PLL system design
- Tyler Bibus:
    - Simulation integration
    - Get Zephyr devices running using the conductor to create and step them.
    - Further design document improvements based on advisor feedback. Contribute to “Design” portion of the design document.
- Aiden Han-Lindemyer: Continue on refactoring modules. Finalize module implementation.
- Parker Pederson: Make the simulation work. Finish Implementation of HCI.
- Akash Gojuru: Complete the full connection state machine and work on the Python refactoring. Fix the issue to match the correct timing with the Babblesim.
- Seth Klaassen: performing LVS on the VCO layout and verifying it is ready for tapeout

Summary of weekly advisor meeting

Top-Level Updates

- **Software Model:** Add a "software model" phase to the project key to accurately reflect additional steps and demonstrate overall progress.

PHY (Physical Layer)

- **Antenna Metrics:** Provide comprehensive metrics to justify the selected antenna's utility for the final project.
- **Antenna Support:** Clarify the system's capacity to support multiple antennas and provide the technical rationale.
- **BLE Compliance:** Determine if supporting a single antenna meets full BLE compliance standards.
- **Documentation Update:** Standardize phrasing in the documentation to: *"Proposing this antenna(s) with these metrics [insert metrics] for the design."*

VCO & Tapeout Strategy

- **Risk Assessment:** Explicitly classify the inductor-based VCO as a high-priority risk within the design document.
- **Mitigation Plan:** Outline potential issues and corresponding solutions for the VCO risk.
- **October Tapeout:** The proposal to perform a standalone VCO tapeout for testing in October is approved as a risk mitigation strategy. Action required: Coordinate with Collin this week to secure a spot on the tapeout schedule.
- **Feasibility Testing:** This tapeout will validate project viability and identify if components (such as an external VCO or PLL) need to be extracted.
- **IP Verification:** Establish a formal verification plan if utilizing existing IP for the VCO.
- **Final Tapeout:** The target for the final tapeout is CI2612, preferably utilizing Caravan.

Digital

- **Simulation Plan:** The proposed simulation strategy is approved and considered highly valuable. (Note: This section received minimal scrutiny during the meeting due to time constraints).

Design Document & Deliverables

- **Risk Feedback:** Incorporate the provided feedback regarding project risks into the design document.
- **Scope Clarification:** Acknowledge that while utilizing Efabless 2.0 is outside the current project scope, the primary deliverable is the open-source IP, not the physical chip itself. However, the final IP design must remain fully fabricable.