EE/CprE/SE 4910 REPORT 9

4/18/2026 – 4/28/2026

Group number: SD26-10

Project title: Open-sourced Radio Microcontroller for Fabrication

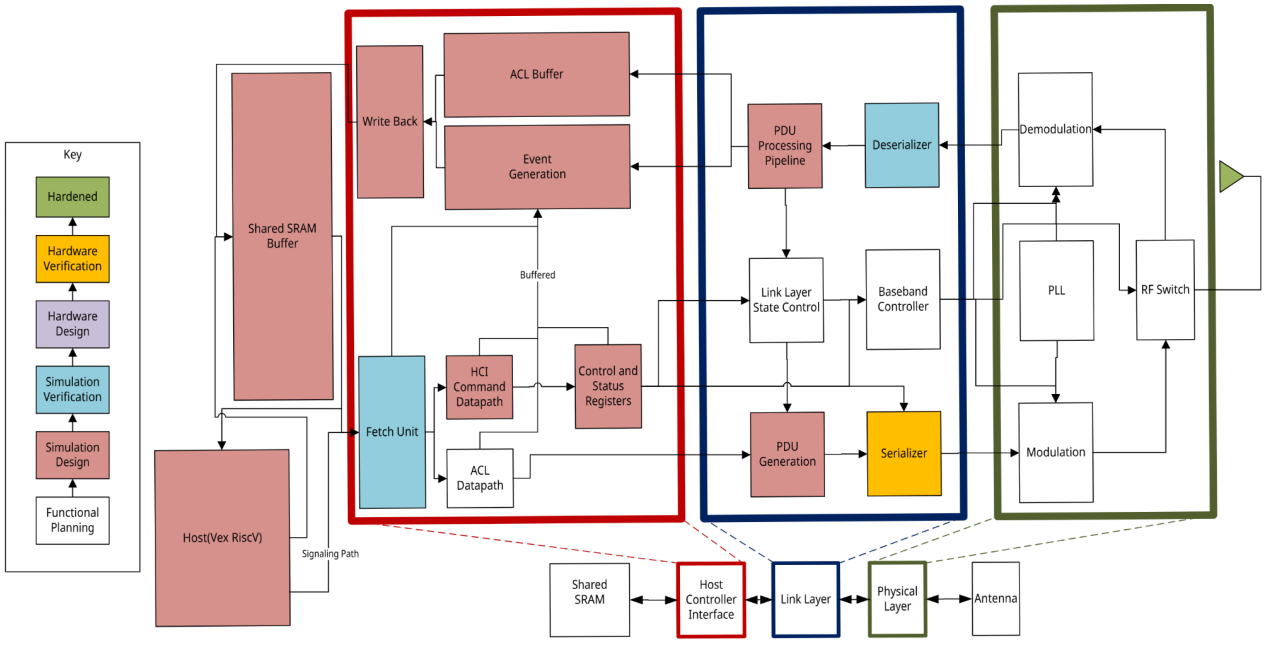
Client &/Advisor: Henry Duwe duwe@iastate.edu

Client/Company/Organization: ISU; ECPE

Team Members:

- *Zane Salti*
- *Jackson Doyle*
- *Daniel Pytel*
- *Tyler Bibus*
- *Aiden Han-Lindemyer*
- *Parker Pederson*
- *Akash Gojuru*
- *Seth Klaassen*

Weekly Summary:



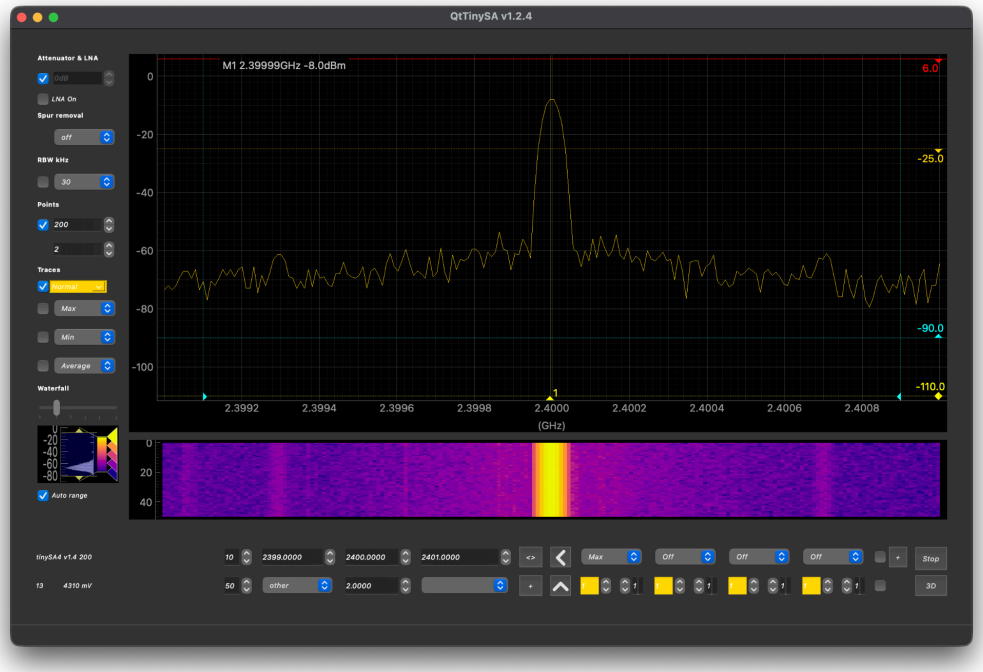
Digital Team Progress:

Good progress has been made on the simulation environment as a basic TX and RX pipeline has been developed and tested against a known-good controller (Zephyr). The sim environment also supports the use of Zephyr devices to test the DUT controller against, which is

how it was confirmed basic advertising and scanning functionality works properly. There are some inaccuracies with the simulation environment modules, for example the HCI datapath also implements the ACL datapath functionality, which needs to be fixed to reflect our block diagram better. The second, and more concerning inaccuracy, is the link layer state control unit, which is empty as the device.py file handles state control through the whole device, which is inaccurate as the link layer determines the actual state.

Past week accomplishments

- Zane Salti: Started with configuring the Ultrascale+ transceiver as a lower frequency transmitter (250 MHz) and then set it up at our desired frequency of 2.4 GHz. Mahmoud Gshash helped me test the 250 MHz configuration with a VNA as well.



Able to shift frequencies on the fly. Here is a frequency shift to 2402 MHz which is the center of channel 37 (the first advertising channel):

As a note, the spectrum analyzer is only plugged into one end of the differential pair of the transceiver for all of these spectrum analyzer screenshots.

The required sdm0/1data value for setting the frequency is:

$$sdmdata = 2^{24} \left(2\,M\,D\,f\,\frac{1}{f_{PLL\ Clk\ In}} - N\right)$$

Where M is QPLL0/1_REFCLK_DIV, D is TXOUT_DIV, and N is FBDIV (some assumptions were made). This was derived from the following formulas given in the Ultrascale GTH user guide and also the fact that the desired frequency is to be half of the line rate (two bits coming out, a 0 and then a 1, makes up a single period for our purposes, but still takes two bits at the line rate):

$$f_{LineRate} = \frac{f_{PLLClkout} \times 2}{D} \qquad \textit{Equation 2-4}$$

Table 2-13 lists the allowable divider values.

Table 2-13: **QPLL0/1 Divider Settings**

Factor	Attribute	Valid Settings
M	QPLL0_REFCLK_DIV QPLL1_REFCLK_DIV	1, 2, 3, 4
N	QPLL0_FBDIV QPLL1_FBDIV	16–160
D	RXOUT_DIV TXOUT_DIV	1, 2, 4, 8, 16
UltraScale+ FPGAs Only		
QPLL_CLKOUTRATE	QPLL0CLKOUT_RATE QPLL1CLKOUT_RATE	2 (Half). This value should not be changed.
SDMDATA	SDM0DATA SDM1DATA	0 – (2^{24} – 1)
SDMWIDTH	SDM0WIDTH SDM1WIDTH	16, 20, 24

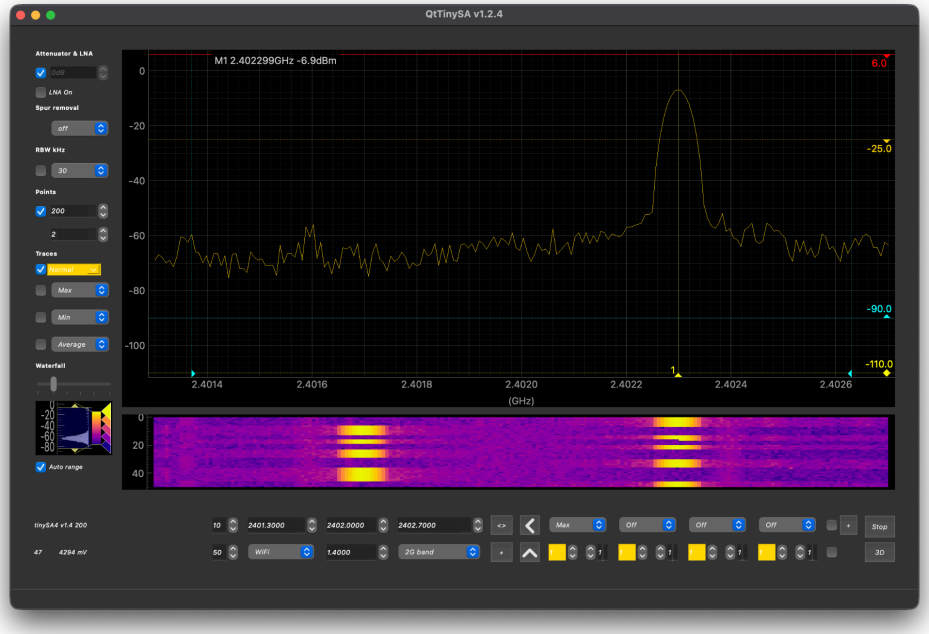
For UltraScale+ FPGAs, the fractional-N feature is supported using the QPLL. Equation 2-5 determines the PLL output frequency when this feature is used.

$$f_{PLLClkout} = f_{PLLClkin} \times \frac{N.FractionalPart}{M \times QPLL\_CLKOUTRATE} \qquad \textit{Equation 2-5}$$

Equation 2-6 shows how to determine the fractional part of the feedback divider presented in Equation 2-5.

$$FractionalPart = \frac{SDMDATA}{2^{SDMWIDTH}} \qquad \textit{Equation 2-6}$$

Got FSK modulation going (slowed down the symbol time by a lot so the spectrum analyzer can differentiate between symbols, otherwise it's too fast to be picked up as distinct symbols):



The advertising attempts didn't get picked up by other BLE devices. I assume this has to do with the fact that the symbol timing was misconfigured (was set up for a little more than 1us) and also that FSK isn't sufficient for BLE (GFSK is necessary). So a gaussian pulse shaping filter was designed. Evaluating and running the computation for this filter in hardware doesn't seem necessary as the inputs are either -1 frequency shift or +1 frequency shift (and in edge cases, 0 frequency shift), so it made more sense to precompute filter output values and use the values in a lookup table. The filter is designed to have 8 samples per symbol and have an input window of 5 symbols. The lookup table can be indexed by the 5 symbols and the specific desired sample, with the relevant active symbol being the middle one, and then the specific sample index being 3 bits concatenated with the 5 bits. The output samples are related to the middle symbol of the input window. Segment of table from Matlab:

	Bit Window	Samples (Normalized)								Frequency Offset								PLL Fraction Offset				
		1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8	1	2	3	4	5
1	"00000"	-1.0000	-1.0000	-1	-1	-1.0000	-1.0000	-1	-1.0000	-2.5000e+05	-2.5000e+05	-250000	-250000	-2.5000e+05	-2.5000e+05	-250000	-2.5000e+05	-107374	-107374	-107374	-107374	-10737
2	"00001"	-1.0000	-1.0000	-1.0000	-1.0000	-1.0000	-1.0000	-1.0000	-0.9999	-2.5000e+05	-2.5000e+05	-2.5000e+05	-2.5000e+05	-2.5000e+05	-2.5000e+05	-2.5000e+05	-2.4999e+05	-107374	-107374	-107374	-107374	-10737
3	"00010"	-0.9996	-0.9980	-0.9912	-0.9678	-0.9044	-0.7661	-0.5249	-0.1882	-2.4991e+05	-2.4951e+05	-2.4779e+05	-2.4196e+05	-2.2609e+05	-1.9152e+05	-1.3123e+05	-4.7056e+04	-107336	-107162	-106426	-103921	-9710
4	"00011"	-0.9996	-0.9980	-0.9912	-0.9678	-0.9044	-0.7661	-0.5249	-0.1882	-2.4991e+05	-2.4951e+05	-2.4779e+05	-2.4196e+05	-2.2609e+05	-1.9152e+05	-1.3122e+05	-4.7043e+04	-107336	-107162	-106426	-103921	-9710
5	"00100"	0.1878	0.5229	0.7572	0.8722	0.8722	0.7572	0.5229	0.1878	4.6954e+04	1.3073e+05	1.8931e+05	2.1805e+05	2.1805e+05	1.8931e+05	1.3073e+05	4.6954e+04	20167	56149	81309	93653	9365
6	"00101"	0.1878	0.5229	0.7572	0.8722	0.8722	0.7572	0.5229	0.1879	4.6954e+04	1.3073e+05	1.8931e+05	2.1805e+05	2.1805e+05	1.8931e+05	1.3073e+05	4.6967e+04	20167	56149	81309	93653	9365
7	"00110"	0.1882	0.5249	0.7661	0.9044	0.9678	0.9912	0.9980	0.9996	4.7043e+04	1.3122e+05	1.9152e+05	2.2609e+05	2.4196e+05	2.4779e+05	2.4951e+05	2.4990e+05	20205	56361	82257	97106	10392
8	"00111"	0.1882	0.5249	0.7661	0.9044	0.9678	0.9912	0.9980	0.9996	4.7043e+04	1.3122e+05	1.9152e+05	2.2609e+05	2.4196e+05	2.4779e+05	2.4951e+05	2.4991e+05	20205	56361	82257	97106	10392
9	"01000"	-0.1882	-0.5249	-0.7661	-0.9044	-0.9678	-0.9912	-0.9980	-0.9996	-4.7056e+04	-1.3123e+05	-1.9152e+05	-2.2609e+05	-2.4196e+05	-2.4779e+05	-2.4951e+05	-2.4991e+05	-20211	-56361	-82257	-97106	-10392
10	"01001"	-0.1882	-0.5249	-0.7661	-0.9044	-0.9678	-0.9912	-0.9980	-0.9996	-4.7056e+04	-1.3123e+05	-1.9152e+05	-2.2609e+05	-2.4196e+05	-2.4779e+05	-2.4951e+05	-2.4990e+05	-20211	-56361	-82257	-97106	-10392
11	"01010"	-0.1879	-0.5229	-0.7572	-0.8722	-0.8722	-0.7572	-0.5229	-0.1879	-4.6967e+04	-1.3073e+05	-1.8931e+05	-2.1805e+05	-2.1805e+05	-1.8931e+05	-1.3073e+05	-4.6967e+04	-20172	-56149	-81309	-93653	-9365
12	"01011"	-0.1879	-0.5229	-0.7572	-0.8722	-0.8722	-0.7572	-0.5229	-0.1878	-4.6967e+04	-1.3073e+05	-1.8931e+05	-2.1805e+05	-2.1805e+05	-1.8931e+05	-1.3073e+05	-4.6954e+04	-20172	-56149	-81309	-93653	-9365

A 256 entry table (2^5 * 2^3) may be a lot thicker than desired or necessary. A 5 symbol window can be reduced to 3 symbol window to reduce the lookup table (for example, it seems that the output samples from x010y are similar to each other for any x and y, so there might not be benefit in considering a 5 symbol window). Also, there seems to be symmetry in the complements which can allow us to reduce it further (2^3 * 2^3 = 64).

A SystemVerilog module has been made to, at compile time, compute the lookup table contents to allow for easy changing of parameters (for example, say the transceiver's TXOUT_DIV attribute changes; instead of recomputing everything and putting in the file, it can take in that value and at compile time calculate the necessary values). The values of the lookup table are offsets in the form/scale that the sdm0/1data value of the transceiver expects. From the earlier formula, the following formula was derived for finding the sdm0/1data offset values:

$$sdmdata_{offset} = 2^{24} \left(2\ M\ D\ f_{offset} \frac{1}{f_{PLL\ Clk\ In}}\right)$$

- Jackson Doyle: Continued work with simulink. Had a conversation with Dr. Neihart to assess direction of project and address possible problems/process issues we may face specifically in regards to SKY130. Neithart is a strong supporter of taking any inductor based components off chip in order to get better performance. (Q factor)
- Daniel Pytel: Discussed implementation aspects with Dr. Neihart. Attempted to get found VCO to tapeout, with limited success.
- Tyler Bibus: Added support for Zephyr devices in our simulation environment to test our devices against. Added advertising via a basic TX pipeline and testing with a Zephyr scanner listening for the advertising packets. Then added scanning via a basic RX pipeline and tested it with a Zephyr advertiser to send out packets, which were able to be received by bumble. The devices could communicate with each other as well through BabbleSim to emulate a wireless environment.
- Parker Pederson: Removed fetch unit and shared ram buffer after determining that buffering gives no benefit in our particular use case. Buffering is already done internally to the host thus buffering it additional gains us nothing.
  Rebuilt simulation in python to previous state of simulation before refactor.
- Aiden Han-Lindemyer: HCI bug fixes and test cases, worked on python refactoring.
- Akash Gojuru: Implemented standby, Advertising, scanning and Initiating states. These states are fully working right now.
- Seth Klaassen:debugging VCO gds file, errors with inductor otherwise working

Pending issues

- Zane Salti: Need to test advertising with the gaussian filter.
- Jackson Doyle: Need to implement more "realistic" functionality in simulink model.
- Daniel Pytel: No inductor.
- Tyler Bibus: Need to integrate Parker's LL state controller and fix some sim alignment issues with block diagram. Most of this will revolve around moving some functionality from one component to another.
- Aiden Han-Lindemyer: Test cases for connection state is still work in progress.
- Parker Pederson: Digital simulation still has slight misalignment with block diagram even though functionality is matched closely.
- Akash Gojuru: Connection state (partially working), have a issue with data transfer timing issue after connection

- Seth Klaassen:unable to get working inductor, may have to move RF sensitive parts off chip

Time Tracking

This report is over a week to have it end at the deadline (as this is supposed to be the last report of the semester).

NAME	Hours this time frame	HOURS cumulative
Zane Salti	17	83
Jackson Doyle	10	60
Daniel Pytel	12	48
Tyler Bibus	11	56
Aiden Han-Lindemyer	10	51
Parker Pederson	11	54
Akash Gojuru	12	54
Seth Klaassen	10	54

Comments and extended discussion

Plans for the upcoming week

- Zane Salti: Test advertising with the gaussian filter and prepare for the final presentation.
- Jackson Doyle: Prepare for faculty presentation and continue work as usual
- Daniel Pytel: Faculty presentation preparation, reassess VCO.
- Tyler Bibus: Prepare for faculty presentation, design document, and SD website. Align the sim environment with our top level module and prepare additional documentation before deliverables to the faculty advisor.
- Aiden Han-Lindemyer:Preparer final presentation and design document.
- Parker Pederson: Prepare for faculty presentation and slightly refactor simulation.
- Akash Gojuru: finish connection state and work on the presentation.
- Seth Klaassen:Prepare for the faculty presentation, rework plan for components requiring inductors

Summary of weekly advisor meeting

We discussed plans moving forward for the analog design. We discussed the previous meeting with Niehart who expressed concerns about the ability of the on chip inductor to function effectively. Potential mitigations were discussed including moving the inductor from the LC VCO off the chip. This is not atypical for VCO design on older processes. Overall simulation architecture for the analog team was discussed with Niehart noting that simulation ADC and DAC components add more simulation time for little gain. Tapeout progress was discussed as well as how integration with the rest of tapeout will proceed.