EE/CprE/SE 4910 WEEKLY REPORT 4

2/28/26 – 3/6/26

Group number: SD26-10

Project title: Open-sourced Radio Microcontroller for Fabrication

Client &/Advisor: Henry Duwe duwe@iastate.edu

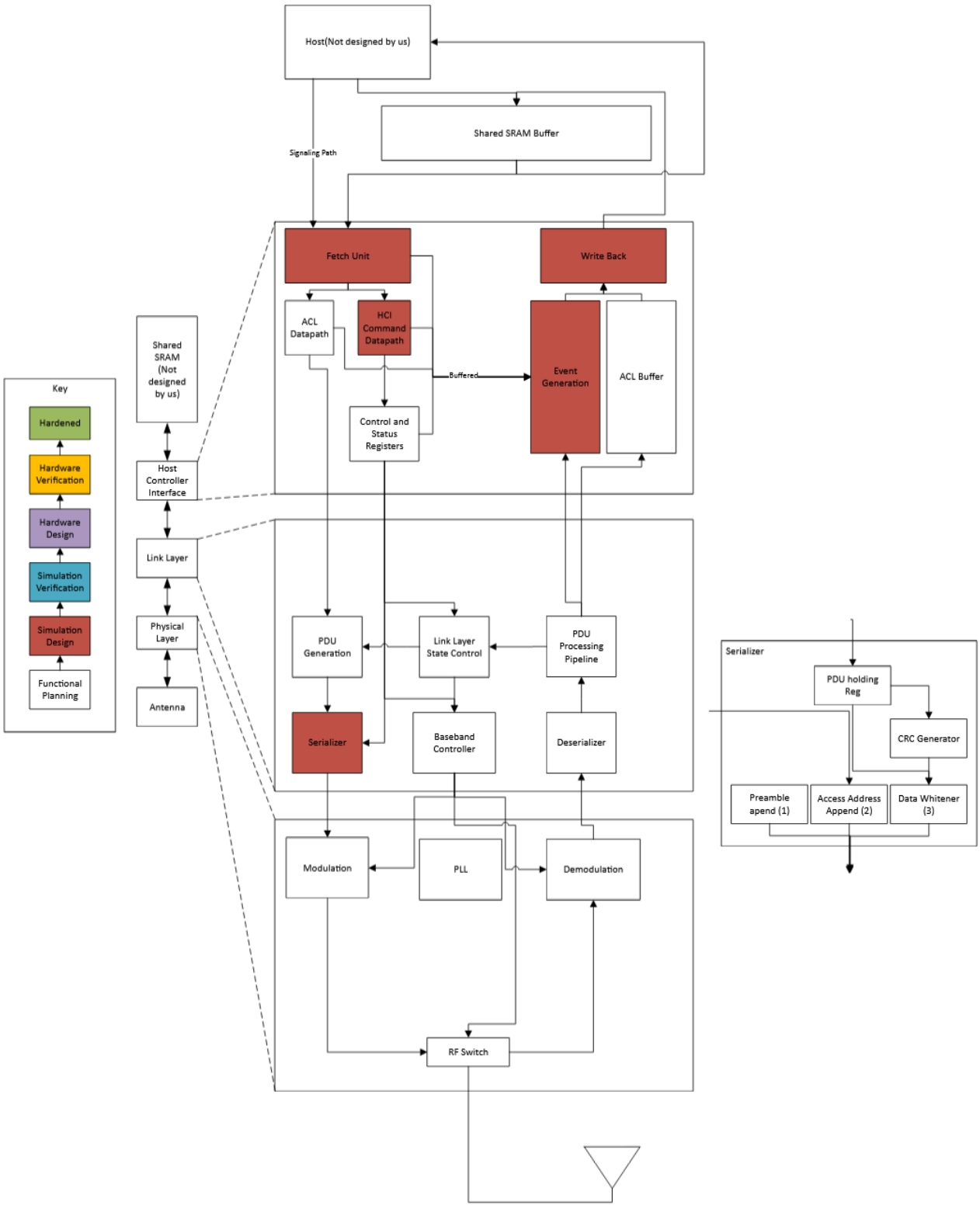
Client/Company/Organization: ISU; ECPE

Team Members:

- ***Zane Salti***
- ***Jackson Doyle***
- ***Daniel Pytel***
- ***Tyler Bibus***
- ***Aiden Han-Lindemyer***
- ***Parker Pederson***
- ***Akash Gojuru***
- ***Seth Klaassen***

Weekly Summary:

Top Level Diagram:

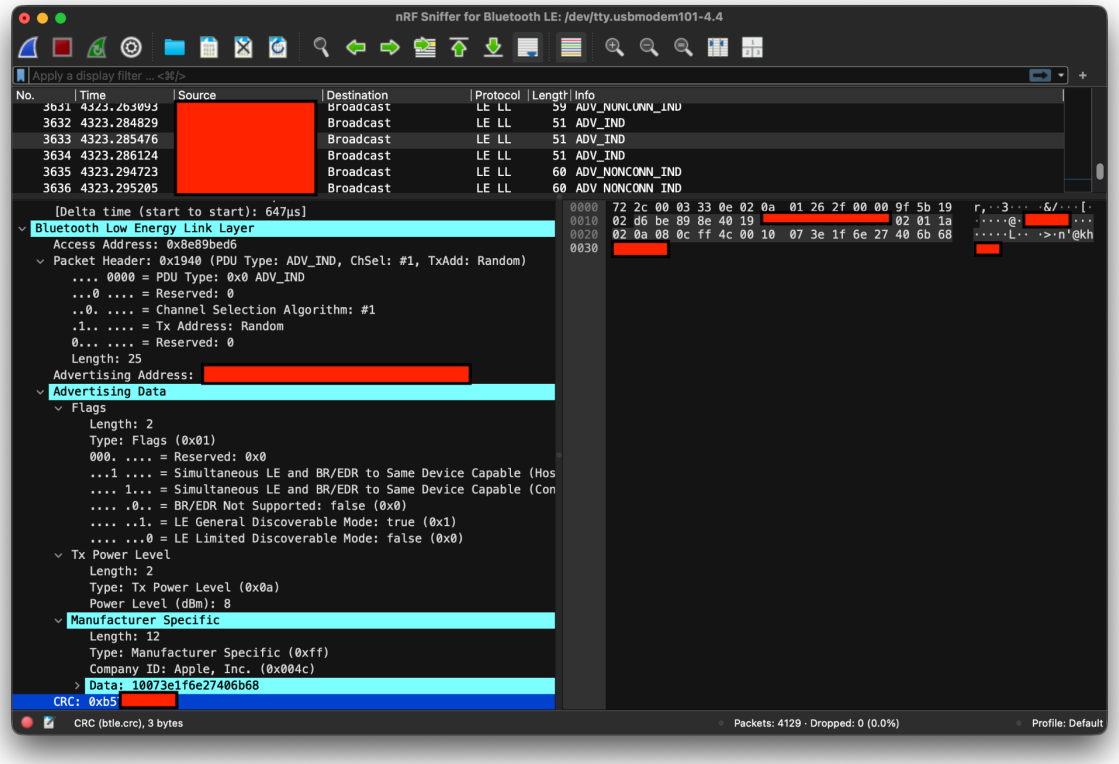


The purpose of this diagram is to create a visual representation of all components in the system and to track their development as the project progresses.

Generally the process for creating a component is to first simulate it using the bumble-babble stack. Then to develop the hardware and match it against the results generated by the simulation.

Past week accomplishments

- Zane Salti: Finished development and verification of the CRC hdl module. Different online CRC calculators were giving conflicting results so a nRF52840 DK (borrowed from Salah Nasriddinov) was used to sniff BLE packets (with this) and the relevant CRCs in those packets were used as a ground truth for verification of the CRC hdl module as well as verification of the assumed algorithm in python.
  Snippet from Wireshark capture (source addresses redacted for privacy; the crc is likewise redacted as otherwise you could just bruteforce the 6 byte advertising address until the crc matches up):



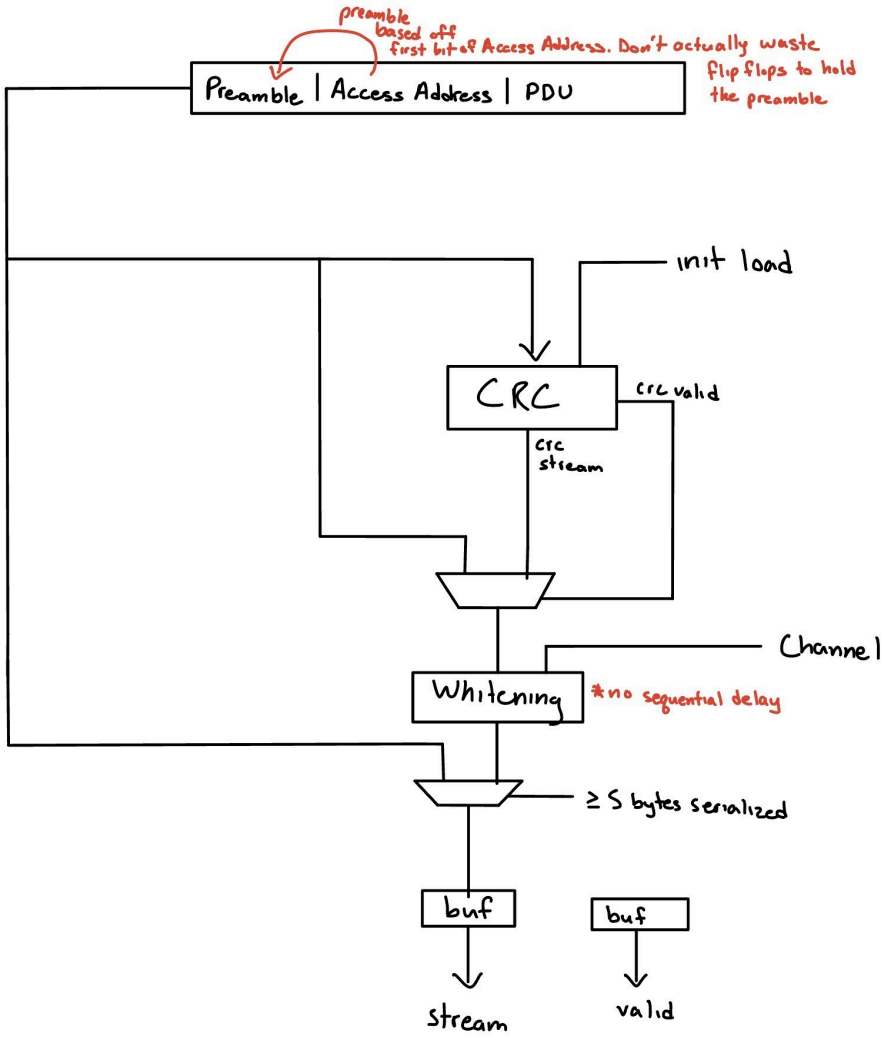
From CRC hdl testbench:

```
# True CRC: 301062. Our CRC: 301062
# Stream looks good.
# Another PDU
```

```
# True CRC: 1b7d2f. Our CRC: 1b7d2f
# Stream looks good.
# Finishing...
```

Implemented the whitening hdl module (not tested yet).

Worked on the serializer architecture design. Preamble is followed by Access Address which is then followed by a whitened PDU which is then followed by a whitened CRC of the PDU:



- Jackson Doyle: Began PLL architecture carryover and feasibility verification. Notably, researches the viability of reusing the prior groups architecture for the VCO. This architecture was primarily composed of a ring oscillator and as such should be fairly simple to adapt and create in the toolflow.
- Daniel Pytel: Set up a meeting with Dr. Neihart for the PHY team to help scope. Began working on an associated presentation to contextualize the project for other advisory meetings. Continued assessing previous group's design, and worked with the rest of the PHY team in realizing the ring oscillator architecture.
- Tyler Bibus: Set up my account on the virtual machine. Installed BabbleSim on VM and ran the tutorial example. Created a more streamlined version of our slide deck for our weekly advisor meeting based off advisor feedback.
- Parker Pederson: Installed Bumblesim on the VM and started the simulation repo. Made simulation scripts to allow for easy tool use for other team members. Created a large top

level diagram to track progress on the project. Was able to decode and respond to a request complete to the simulated host.
- Aiden Han-Lindemyer: Received VM from ETG and set up with up to date Python version so Bumble can be installed and used. Connected and used bumble to run advertisement examples with success.
- Akash Gojuru: I received the VM from ETG, updated it with the latest Python version so Bumble can be installed and wrote the PDU generation code for Verilog.
- Seth Klaassen: reading reports of past PLL architecture reports as well as documentation on the toolchain from the another senior design group

Pending issues

- Zane Salti: Serializer hdl needs to be implemented. Whitening hasn't been tested.
- Jackson Doyle: Need to begin testing of the VCO in xschem. The first step to doing so is ideally creating a working inverter, and from there creating a working ring oscillator. Need to meet with Neihart
- Daniel Pytel: Still need to finish presentation, partially at a standstill until the meeting.
- Tyler Bibus: Still learning more about BabbleSim, with a need to expose the logic of the examples given to learn from and base off.
- Aiden Han-Lindemyer: Get babblesim set up on my machine and work with examples.
- Parker Pederson: Need to solve asynchronous write from host to sram buffer problem in simulation.
- Akash Gojuru: working on PDU testing and trying Bumble simulation examples.
- Seth Klaassen: get a working model of the RF switch in the toolchain

Time Tracking

NAME	Hours this week	HOURS cumulative
Zane Salti	8	29
Jackson Doyle	5	15
Daniel Pytel	4	13
Tyler Bibus	4	16
Aiden Han-Lindemyer	4	16
Parker Pederson	5	18
Akash Gojuru	3	14
Seth Klaassen	3	18

Comments and extended discussion

Plans for the upcoming week

- Zane Salti: Work on serializer hdl implementation, meet with Neihart, and look at physical hardware solutions for testing the digital Link Layer with (GFSK transceivers, chip PLLs, etc.)
- Jackson Doyle: Meet with Neihart, begin realization of VCO design in toolflow. Hopefully achieve a functional ring oscillator in the toolflow by the time we have our advisor meeting
- Daniel Pytel: Meet with Neihart to set concrete scope for PHY team, possibly reach out to other professors as well.
- Tyler Bibus: Set up simulation scripts for BabbleSim. Study how the example Host and Link Layer function, hopefully exposing lower level state logic.
- Aiden Han-Lindemyer: Start on HCI response commands. Start the acronym index because we have a lot. Work on and run BabbleSim examples.
- Parker Pederson: Finish setting up the sram buffer simulation. Do basic simulation response for basic HCI commands.
- Akash Gojuru: Implement the CSA1 algorithm and test it, and use Bumble examples to run simulations.
- Seth Klaassen: implement the RF switch in the toolchain

Summary of weekly advisor meeting

Acronym footnotes are highly advised from here on out. Similarly, a glossary will be a useful asset, both for personal reference and for the final design document. The problem statement ought to be modified to orient towards fabrication, and the user descriptions should change accordingly. The division of labor needs to be made more concrete.